Customer Specific Requirements
(ISO/TS-16949)
Semiconductor Commodity

FOR USE BY SEMICONDUCTOR SUPPLIERS

Customer Specific Requirements
(ISO/TS-16949)
Semiconductor Commodity

FORWARD TO FIRST EDITION CUSTOMER REQUIREMENTS (ISO/TS-16949)

SEMICONDUCTOR COMMODITY

The Automotive Electronics Council (AEC) has revised the QS-9000 (second edition) Semiconductor Supplement as an evolution to utilize and align it with the ISO/TS-16949 (second edition) standard as a customer specific requirements document for the semiconductor commodity. As with the QS9000 Semiconductor Supplement, Second Edition, this document coordinates its paragraph numbering with the base document. The comprehensive document for semiconductors becomes this document coordinated with the ISO/TS-16949 standard. Some minor rewording or changes have been incorporated into this document as it evolved from the QS-9000 supplement. For continuity, the forwards to the prior editions of the QS-9000 supplements have been reproduced below.

The AEC is thankful to the Supplier Quality Engineers, Component Engineers and Suppliers to our respective companies that have offered suggestions to improve this document. Thanks also go to the members of the DaimlerChrysler/Ford/General Motors Supplier Quality Requirements Task Force and to Chad Kymal, President of Omnex, for their on-going guidance and direction.

FOREWARD TO SECOND EDITION, QS-9000 SEMICONDUCTOR SUPPLEMENT

The Automotive Electronics Council (AEC) has revised the QS-9000 Semiconductor Supplement for three reasons. First, it has desired to maintain consistency with the third edition of QS-9000. Second, as the QS-9000 Semiconductor Supplement has been used in assessments; questions and suggestions for improvement of the document have been received from auditors and semiconductor companies audited. Third, the first edition was written to recognize that the AEC would be primarily conducting second party assessments of semiconductor suppliers. Now that the majority of the assessments are being conducted by third party registrars, it was determined that the document needed to be strengthened and many of the requirements clarified to guide the auditors and suppliers.

The AEC would like to thank all the Supplier Quality Engineers and Component Engineers in their companies and the many semiconductor company personnel that have made suggestions for improvement of this document. A thanks also goes to the members of the Chrysler/Ford/General Motors Supplier Quality Requirements Task Force for their on-going guidance and direction.

FOREWARD TO FIRST EDITION, QS-9000 SEMICONDUCTOR SUPPLEMENT

The Automotive Electronics Council (AEC) under the guidance of the Chrysler/Ford/General Motors Supplier Quality Requirements Task Force developed **Quality System Requirements QS-9000 Semiconductor Supplement**. The AEC retains control of the document under direction of the Task Force.

The AEC is a cooperative alliance among the parts engineering/components engineering and supplier quality groups of Chrysler, Delco Electronics and Ford. This document is the result of requests from the semiconductor industry to provide a common interpretation and application of the former individual company quality system requirements that have now been standardized by the Task Force.

The AEC has developed these supplementary requirements to QS-9000 to ensure consistency in the quality system assessment processes.

This document:

- Is consistent with the Chrysler/Ford/General Motors Quality System Requirements
- Utilizes the Chrysler/Ford/General Motors Quality System Assessment document and process
- Provides the interpretation of nomenclature specific for the semiconductor industry
- Applies to semiconductor suppliers to Chrysler/Ford/Delco Electronics
- Is designed to aid the semiconductor supplier in implementing an effective quality system
- Assists the supplier in preparation for second party audits

The AEC and Task Force are confident that this supplement, implemented in the spirit of continuous improvement, will enhance quality systems while eliminating redundant requirements, facilitate consistent terminology, and thus reduce costs. In that same spirit, the Task Force and AEC encourage suppliers to suggest how the document and its implementation can be improved.

Document Revision History

Revision	Sec/Par Changed	Change Made
Sept 2, 2002	Entire Document	Initial Release
Jan 12, 2004	7.4.1.2S	Add note above requirement, reword requirement, and reword second note
Jan 12, 2004	7.6.3.1S	Changed from “The organization may choose to……” to “The organization should choose to…..”
Jan 12, 2004	Appendix C. Delphi and Visteon Customer Specific Requirements	Delphi changed division names and reduced divisions from six to five. Visteon deleted all customer specific requirements.
Jan 12, 2004	Key Contacts	Changed email address for Delphi contact
Jan 12, 2004	Document Revision History	Added Document Revision History table prior to Table of Contents.
Jan 12, 2004	Table of Contents	Re-paged the Table of Contents and the rest of the document.

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I Introduction

I.1 Goal

The goal of this document is to assist the semiconductor industry in the application of ISO/TS-16949 (second edition) for the development of fundamental quality systems that provide for continuous improvement, emphasizing defect prevention and the reduction of variation and waste in the semiconductor supply chain.

I.2 Purpose

This customer specific, commodity document provides a consistent interpretation between DaimlerChrysler, Delphi Corporation and Visteon Corporation of ISO/TS-16949 and communicates additional common system requirements unique to the producers of semiconductor devices.

I.3 Approach

This customer specific, commodity document is intended to fully embrace the current release of ISO/TS-16949. It is recognized by DaimlerChrysler, Delphi Corporation, Visteon Corporation, and the semiconductor suppliers that automotive industry language begs consistent interpretation and application. This supplement has been generated by quality and engineering professionals of DaimlerChrysler, Delphi Corporation and Visteon Corporation with considerable assistance from the semiconductor industry.

ISO/TS-16949 together with this customer specific document constitutes the comprehensive requirements document for the semiconductor industry. The two documents shall be used together to comprehend all requirements and definitions.

I.4 Applicability

ISO/TS-16949 and this customer specific document applies to the internal and external suppliers of production and service semiconductor parts and materials. Every clause of ISO/TS-16949 and this customer specific document applies to semiconductor suppliers with the possible exception of design and/or service. These clauses should be carefully analyzed with the customer or registrar to determine applicability to a particular site or activity.

I.5 Implementation

Implementation is based on ISO/TS-16949 with the addition of the customer specific requirements for semiconductor suppliers.

AEC qualification and quality documents are available through the AEC website: www.aecouncil.com. The following AEC Documents are available in software version :

AEC-Q001 Guidelines for Part Average Testing
AEC-Q002 Guidelines for Statistical Yield Analysis
AEC-Q100 Stress Test Qualification for Integrated Circuits
AEC-Q101 Stress Test Qualification for Discrete Semiconductors
AEC-Q200 Stress Test Qualification for Passive Components

It is suggested that the AEC documents be implemented as part of this document as referenced within.

Semiconductor Assembly Council (SAC) documents are available through the SAC website. Open "www.sacouncil.org," select "SAC STANDARDS" and follow the directions for members or nonmembers.

The following SAC Standards are available and are suggested for use and implementation as referenced within this document:

SAC-STD-001 Certification Standard
SAC-STD-002 Audit Standard
SAC-STD-003 Package Qualification Standard
SAC-STD-004 Process Control Standard
SAC-STD-005 Product/Process Change Standard
SAC-STD-006 Documentation Control Standard
SAC-STD-007 Quality System Checklists

The following reference manuals are required as part of the implementation as refereneced within this document:

These documents are available through AIAG 01-248-358-3003. In Europe, contact Carwin Continuous at 44-1708-861333.

Measurement Systems Analysis Reference Manual
Statistical Process Control Reference Manual
Potential Failure Mode and Effect Reference Manual
Production Part Approval Process
Advanced Product Quality Planning and Control Plan Reference Manual

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3.1.5S Laboratory

For laboratory scope, laboratories are those facilities that perform reliability, qualification or durability testing to the requirements of a customer documented specification or calibration of measurement equipment.

4.2.4.1S Control of records

Where characterization records and design of experiments (DOE) are used to demonstrate conformance, the organization shall maintain those records for the production and service life of the part plus one full calendar year or until characterization for the part or family of parts has been updated.

Field and customer problem and failure analysis reports shall be retained for three years.

5.4.1.1S Quality objectives - supplemental

See 7.3.7S for guidance on business plans and quality objectives.

6.2.2.2S Training

Process steps that require operator certification will be identified and operators certified. These operators shall be periodically re-certified.

6.4.2S Cleanliness of premises

The following environmental and housekeeping items shall be controlled where appropriate:

- ESD controls and discipline
- Airborne particles
- Chemical particle count
- Machine particle count
- Humidity

- Temperature
- General workstation cleanliness
- Water resistivity
- Robing requirements and discipline

7.1S Planning of product realization-Supplemental

The product realization planning shall include processes from the incoming material through shipping and warehousing. Failure mode and effects analysis and control plan documents shall include these processes.

NOTE: The organization should consider the entire supply chain in product realization planning. This should encourage the use of FMEA, Control Plan, and other preventive tools.

Product realization planning shall be extended to include material movement between controlled and contracted sites, such as :

- Fabrication to assembly
- Assembler to test house

The intent of this activity is to establish a customer/supplier relationship between the sending and receiving organizations to facilitate requirements definition and process mistake proofing.

- The receiving and sending organizations shall agree upon performance/capability requirements that as a minimum establish product/process expectations, timing and support requirements.
- Feasibility concerns shall be documented and a plan developed to remove the feasibility concerns with special attention to external and internal customer concerns**.**

7.1.4S Change control

Effects of process changes shall be verified by before and after characterization of the appropriate device parameters. This applies to both proprietary and nonproprietary designs.

7.2.1.1S Customer-designated special characteristics

If the customer does not identify any special characteristics, the organization shall identify those process parameters or product characteristics that are critical to proper operation of the product.

7.2.2.2S Organization manufacturing feasibility

The feasibility analysis shall include a compatibility review of current design rules, critical process capability and design/process FMEA with manufacturing personnel.

Conformance to engineering requirements shall be demonstrated by providing process and/or product characterization data. Statistical data shall show significant process and product special characteristics are capable or have a customer approved action plan.

7.3.1S Design and development planning

For custom or application specific parts, the organization shall review with and, as appropriate, obtain customer concurrence at appropriate stages of design and development. Design process effectiveness is indicated by evidence of first pass design success.

7.3.2(d)S Design and development input

Device and process simulation model robustness shall be reviewed periodically to assure design and process compatibility. The organization shall have a documented procedure defining the review methods and frequency. This procedure shall include the extraction of key semiconductor parameters to verify process to model robustness.

NOTE: For semiconductor organizations, it is not required that CAD/CAE systems be capable of two way interface with customer systems unless this capability is requested by the customer for specific parts.

When a new process or technology is being designed, the organization shall consider the customer product life cycle vs. the process or technology life cycle being developed. When a technology or process is identified as becoming obsolete, the organization shall notify the customer and develop plans to manage the obsolescence. See also 7.3.7 S.

7.3.3S Design Output

The organization shall be able to produce data that:

- device packaging meets customer requirements
- transportation packaging meets customer requirements

Parameters which are specified as “guarantee by design” shall be identified in the DFMEA. The organization shall document the method used to guarantee such a parameter (i.e., correlated to other tested parameters, controlled by process controls) both at design and over time.

NOTE: Due to the nature of semiconductors, where multiple parts come from a common family based on common technology and processing, family DFMEAs are acceptable. Specific design differences for parts within the family may require supplements to the family DFMEA.

The organization shall have a documented method for correlating design and product requirements to process target values. For example, process data may be used to verify design and product simulations.

7.3.3.2S PFMEA

PFMEAs shall consider processes from incoming material receipt to shipping and warehousing. Mistake proofing tools shall be used to prevent mixed material, wrong labeling and other common shipping, logistics and storage errors.

NOTE: Due to the nature of semiconductors, where multiple parts come from a common family based on common technology and processing, family PFMEAs are acceptable. Specific process differences for parts within the family may require supplements to the family PFMEA.

NOTE: The organization should consider the entire supply chain in product realization planning. This should encourage the use of FMEA,Control Plan, and other preventive tools.

7.3.5.S Design and development verification

The organization shall be able to produce data showing that each fabrication process has been characterized to the corners of signficant characteristics of the process or per customer requirements.

The organization, when required as part of design verification, shall:

- obtain customer approval for design and process characterization
- obtain customer approval for certified test application
- supply prototypes for evaluation in the application

7.3.6.1.S Design and development validation

A major component of design validation in the semiconductor industry is qualification testing.The organization shall:

- Have customer approval for qualification tests, sample sizes, and test requirements,
- Have a qualification plan (whether qualification is internal or subcontracted) that includes process capacity, reliability test capacity, schedule, and test equipment,
- Have access to adequate laboratory equipment with which device failures may be analyzed, and
- Obtain customer concurrence for problem analysis related to qualification test failures and corrective actions.

Design validation in the semiconductor industry may also include reliability monitoring. Design rule modification should result when the design is no longer robust as indicated by the reliability monitor results.

NOTE: The following are examples that indicate continuous improvement: wafer level reliability; dynamic dielectric breakdown; test to failure.

The organization shall obtain customer concurrence for problem analysis related to design validation test failures and corrective actions.

7.3.7 S Control of design and development changes

The control of design and develop changes shall include long term planning for process changes and technology development. The plan shall include:

- technology roadmaps,
  - ⇒ wafer fabrication/processes
  - ⇒ assembly/packaging
  - ⇒ obsolescence
- quality roadmaps, and
- product development roadmaps.

Whenever product or technology obsolescence plans are made or updated which affect any parts previously purchased by a customer; that customer shall be notified of the obsolescence plans.
(See also 5.4. for business plan requirements)

NOTE: The fact that the technology within the semi-conductor industry moves much faster than automotive product life cycles, the semi-conductor organization's business plan must include the needs of the automotive customer. This should include obsolescence plans consistent with automotive life cycles.

7.4.1S Purchasing process

The organization shall assure that supplier facilities and personnel which perform qualification testing or failure analysis meet customer specific requirements.

NOTE: Purchased products include products and services that affect customer requirements such as subcontract assembly, fab, test, software services, device programming, warehousing or other similar processes that may affect customer product realization.

7.4.1.2S Supplier quality management system development

NOTE: With the increased use of external manufacturing (foundries), the intent is that both internal and external semiconductor manufacturing sources must meet the requirements of ISO/TS-16949:2002 and this document.

Semiconductor organizations who choose to subcontract foundry, assembly and/or test processes shall assure those suppliers conform to the requirements of ISO/TS-16949:2002, including the Semiconductor Commodity Specifics. Conformity may be verified by:

- Third party registration to ISO/TS-16949: 2002
- Certification by the Semiconductor Assembly Council (SAC)
- Customer conducted or approved audits

Organizations should contact their customers to determine which of the above methods are acceptable.

NOTE: All other supplier development defaults to the ISO/TS-16949:2002 requirements.

7.4.3.1S Incoming product quality

The organization should identify the incoming material characteristics that significantly impact their processes. The organization should communicate those characteristics to the supplier.

Where supplier's submitted statistical data is used as a control method, the supplier's SPC methods shall conform to requirements in the **Statistical Process Control** and the **Measurement Systems Analysis** reference manuals.

7.5.1.1S Control Plan

Control plans shall include processes from incoming material through shipping and warehousing.

NOTE: Due to the nature of semiconductors, where multiple parts come from a common family, based on common technology and processing, family Control Plans are acceptable. Specific process or control differences for parts within the family may require supplements to the family Control Plan.

NOTE: Prototype - During the early phases of integrated circuit development, the "prototype" version may not have the required physical, dimensional or material properties of the specified final part. Additionally, the quantities of IC prototype parts are usually small, making the classic concept of control plans inappropriate for this commodity. For instance, the prototype may be ceramic rather than plastic, a multi-chip module rather than a single die, or an emulator rather than a packaged die. The prototype

control plan for this stage of the design development process is developed between the user (customer)

and the organization so that the concerns and expectations of the customer and an agreed upon method of compliance from the organization are documented.

NOTE: Pre-Launch - The pre-launch control plan is a transitional document which bridges between the prototype and production control plans. It is similar to the production control plan in that it includes physical, dimensional and material properties and the testing required for component qualification of the production process. It normally occurs after DV (design verification) and before production ramp-up. The pre-launch control plan also includes the preliminary production control plan for process control to ensure the qualification build and test of production intent components is as close to the final production process and controls as possible.

NOTE: Process control is used to identify special causes of variation and trigger appropriate action. One such action would include incorporating those special causes into the D/PFMEAs, if those causes are not already included.

NOTE: Production - The production control plan is a living document which includes SPC node points for special characteristics identified in the design and process FMEA. It also includes the lessons learned in the execution of the pre-launch control plan.

7.5.1.2S Work instructions

Work instructions shall include or reference as appropriate:

- Automatic test equipment programs and hardware (including device interface board and cabling)
- Data entry to log sheets or computer system
- Golden units (when applicable) and required usage frequency
- Where special characteristics are flagged on the control plan, the reference operator instructions shall be noted

7.5.1.5S Management of production tooling

Along with equipment, preventive maintenance shall also apply to:

- Probe cards
- Tester contacts

The organization shall establish and implement a management system for:

- Device handling equipment
- Test fixtures
- Software
- Testers
- Photo masks

That management system shall include measures of effectiveness for:

- Operational efficiency (uptime efficiency)
- Maintenance to schedule
- Maintenance adjustments consistent with equipment utilization
- Tool change programs for perishable tools such as bond tools, wafer saws, or other wear items that may have a deleterious effect on product that is processed

Tooling management for semiconductors shall include tools that change the form, fit, or function such as:

- Mask sets (not a repairable item)
- Wire bond capillaries
- Trim and form and singulation tools
- Molds
- Probe cards, contactors, and electrical test fixtures

7.5.3S Identification and traceability

The organization shall be able to trace product (incoming, in-process and shipped materials and test data) forward and backward within 24 hours. This time period starts when the organization is notified of a problem with trace code information and ends when the appropriate information is supplied to the customer. As a minimum, the organization shall be capable of identifying and tracing process lots and bill of material items. The time period for traceability may be modified by specific customer requirements.

NOTE: Traceability is used by the customer for risk abatement and containment. Along with the parts being manufactured, it should include the incoming material, the equipment used, test data, and SPC data throughout all steps in the process from receiving through shipment to the customer. Backward traceability is the ability to take the product lot identification (preferably the part marking) and move back into the process to assist in determining the point of origin of a problem and the extent of the root cause. Forward traceability is the ability to move from the point of root cause origin to identify all product affected.

NOTE: Evidence of continuous improvement may include:

- Use of a world-wide accessible computer tracking system which provides on-line status of all product in process
- Use of a machine-readable product identification system
- Mistake proofing techniques should be used to prevent mixing or misprocessing (at both internal operations as well as customer shipments) of production materials

Examples:

- bar coded lot travelers
- bar coded wafer trays
- bar coded entry of process recipes
- color coded tubes for rejects
- automatic clearing of test shuttle mechanism
- automatic printing of bar code labels to match only the number needed
- only one lot at a time at final packaging and shipping

7.5.4S Customer property

The organization shall adequately protect customer supplied product from damage and deterioration caused by environmental conditions (i.e., oxidation and contamination) and handling (i.e., mechanical damage and ESD). The supplier shall have a documented method of inspecting or detecting signs of damage or deterioration caused by environmental or handling conditions. When value added operations

are performed by a subcontractor, the organization shall provide guidelines for the protection of product from handling damage and environmental contamination deterioration.

Where the customer supplies software such as ROM codes, net lists, test vectors or other such intellectual property, the organization shall have a documented method to ensure protection and/or security of the customer's intellectual property rights, verification of correct software in the delivered product, and archiving control.

NOTE: This section refers to the control of materials by both internal (captive fab, assembly, and test facilities) and external (subcontract) companies. The term "Customer-Supplied Product" applies to both product moving between sites (i.e. fab to assembly to test) and items supplied by the customer for design or testing purposes (i.e. correlation samples, customer products).

This clause refers to internal transfer of materials from one manufacturing location to another, as well as to the customer**.**

NOTE: Handling methods that prevent damage or deterioration to product may include:

- Prohibiting the use of tweezers in wafer fab,
- Discarding product which jams in handling equipment,
- Covering wafer boat carriers to reduce contamination,
- Using appropriate finger cots or gloves.
- Using proper ESD control (equipment, personnel, and carts).
- Appropriate equipment to protect die, leadframes, wirebonds, and lead coplanarity during processing and inspection.

The organization shall use appropriate storage methods for prevention of product damage.

NOTE: Examples are:

- ESD controls,
- N_2 or dry air cabinet for exposed wafers and moisture sensitive packaged parts,
- die bank controls,
- temperature and humidity controls.

NOTE: The nature of many semiconductor products requires periodic testing to detect degradation; for example, product solderability.

Transportation packaging shall meet ESD requirements, make proper use of dry pack/desiccant, and prevent physical damage.

7.5.5.1S Storage and inventory

NOTE: The goal is to minimize inventory, however, the long process cycles and lot processing of semiconductors generally makes one-piece flow and an order driven process impractical. For semiconductor processing, actual vs. theoretical cycle time and low work in process (WIP) are good indicators of a managed process.

7.6S Control of monitoring and measuring devices
When a test system setup is accomplished, master/golden units shall be used to verify test system integrity. These golden units shall be distributed within the specification limits, and some golden units shall be outside test limits. The supplier shall safeguard control standards and/or golden units to prevent degradation. Evidence shall be available to demonstrate the frequency and result of the set up.

NOTE: Where golden units or other in house test verification units are used, it is recommended that the master or the golden units be charted. Reaction limits on such charts should be chosen using statistical methods.

NOTE: It is recommended that test software have 100% test coverage for the device under test and interface circuit board.

7.6.1S Measurement system analysis

In order to provide adequate measurement system discrimination, for measurement equipment used to measure special characteristics, the apparent resolution of the equipment shall be at most one-tenth of the total process six sigma standard deviation. (Reference **Measurement System Analysis**, Section 2.)

NOTE: Suppliers are expected to obtain value added state of the art measurement equipment. There are rare instances when a special characteristic distribution is very narrow and the state of the art equipment cannot discriminate at the stated level The supplier should repeat gage R&R studies when warranted by measurement system change (including operator) and have a systematic method to improve gaging.

The supplier measurement system studies shall be per **Measurement System Analysis** reference manual and consistent with process Cp.

7.6.3S Laboratory requirements

Internal and external laboratories selected by the organization for qualification testing shall be capable of performing the tests required in **AEC-Q100** and/or **AEC-Q101** applicable to the types of parts being supplied. The tests outlined in these documents are those typically accomplished as part of PPAP.

7.6.3.1S Internal laboratory

If the internal laboratory is used for engineering development and/or failure analysis, then the production use equipment and processes must be clearly identified. The organization should chose to use laboratory scope statements to document the qualification, production equipment and measurements performed.

NOTE: Laboratories may be used for production measurement of process parameters such as phosphorous content, plating thickness/composition, and chemical analysis of materials.

8.2.2S Internal Audit

The organization's internal audit program shall include:

- Clean room controls
- ESD controls
- Proper handling of masks, wafers, gases, and product
- Corrective actions and effective implementation required from problem analysis reports
- Timely completion of analysis reports including containment, verification, and root cause and corrective action identification

8.2.4S Monitoring and measurement of product

Where visual inspection is used, the organization shall maintain:

- Appropriate lighting for evaluation areas
- Appropriate visual aids (e.g. photos or examples of good and bad product)
- Adequate inspection aids and evaluation equipment
- Verification that personnel performing visual evaluation are competent

If stress testing is employed as a reliability improvement technique, appropriate reliability data shall demonstrate that no part degradation occurs. When guard banding is used to assure omitted test compliance, the organization shall document statistical justification for guard banding methodology.

Correlation and guardband limits are often used to assure compliance to omitted, customer specified, electrical parametric tests. Such guardband limits shall statistically provide a Cpk of 1.67or greater.

The above reliability and statistical data shall be supplied to the customer upon request.

Organizations shall perform lot acceptance testing if required by the customer.

Organizations shall conduct audits of final packaged product to verify conformance to packaging and labeling requirements.

NOTE: Due to semiconductor packaging techniques, it is not required that part testing be performed on parts packaged for shipping unless specifically required by the customer.

NOTE: Unless specified in customer documentation, customer approval of visual acceptance criteria for semiconductor processes is not required.

NOTE: The organization is encouraged to protect the customer by establishing and using part average testing and/or utilizing a maverick lot program. (See AEC-Q001, Guidelines for Part Average Testing and AEC-Q 002 Guidelines for Statistical Yield Analysis)

8.3.1S Control of nonconforming product-supplemental

Non-conforming product should be removed from production and immediately placed in a status that prevents reintroduction into the production flow.

8.3.2S Control of reworked product

When a rework process is established it shall be statistically validated that the reworked product is as reliable as non-reworked product.

NOTE: Continuous improvement may be demonstrated by virtual elimination of rework/redo and significant reduction in scrap rates.

8.5.2S Corrective action

The organization shall have a system to track customer problem analysis completion time.
Unless otherwise agreed to with the customer, the organization shall provide:

- containment within 24 hours,
- problem verification within 48 hours,
- root cause identification and a corrective action implementation plan within 10 calendar days.

NOTE: The goal of containment is to have certified product at the customer in 24 hours.

NOTE: These time periods start when the organization is notified of a problem with trace code information and ends when the appropriate information is supplied to the customer.

The organization shall provide adequate facilities for complete semiconductor failure analysis. If the organization cannot perform such analyses, services shall be contracted from an adequate external laboratory, or upon special arrangements, provided by the customer.

Analytical equipment used for failure analysis shall be included in a preventive maintenance and calibration control.

Appropriate organization management shall review problem analysis reports, failure analysis reports, and corrective action prior to submission to the customer.

The organization shall incorporate significant feedback from field return analysis into design rule documentation, design and process FMEAs, and process control plans.

Appendix A: Additional TS-16949 Registration Requirements

A.1 Certificate Requirements

Certificates for semiconductor suppliers shall include wording that indicates that the requirements of the Customer Specific Requirements (ISO/TS-16949) Semiconductor Commodity were included.

A.2 Semiconductor Supplier Registration

Semiconductor suppliers are not typically direct suppliers to OEMs. Some tier one suppliers to the OEMs have a customer specific requirement for tier 2 suppliers to be third party registered to ISO/TS16949. Through this, the AEC members encourage all manufacturing locations of semiconductor suppliers to become registered or certified in accordance with their specific requirements. This locations may not ship directly to OEM or Tier 1, but provide a significant portion of the manufacturing process. As such, they should be included in the registration process.

Appendix B: Code of Practice for Quality System Certification Bodies/Registrars

B.1 Audit planning

During the audit planning, to assure that all relevant processes and support functions are included in the audit of a semiconductor supplier, the audit team should use a site map, floor plan, and process flow diagram to determine flows for raw materials (gases, DI water, chemical supply), tooling shops (molds, masks, trim and form, probe cards), and other support functions. These functions shall be included in the site audit as appropriate.

B.2 Technical member of the audit team

At least one member of the audit team shall have relevant semiconductor industry experience.

B.3 Instructions to Suppliers Concerning Third Party Registration

For semiconductor suppliers, the registration certificate shall include wording to indicate that the requirements of the **Customer Specific Requirements** (**ISO/TS-16949) Semiconductor Commodity** were included.

B.4 Implementation of the ISO/TS-16949 System

Semiconductor suppliers typically have multiple sites, which utilize centralized purchasing, design, and other functions. It is recommended that a "high level" process flow description or diagram be made to determine the locations of the key functions. If site-by-site registration is selected, the centralized support functions should be audited first so that manufacturing site registration can be completed on a site-by-site basis.

Appendix C. Customer-Specific Requirements

DaimlerChrysler – Specific Requirements

Annual layout inspection is not required for semiconductor devices with the exception of parts which have custom lead forming.

The Process Sign-Off line speed demonstration (line 19 in the PSO 3rd Edition) and BSR/NVH (line 21 in the PSO 3rd Edition) are not required for PSO approval.

Delphi Corporation – Specific Requirements

Laboratories used for qualification of semiconductors for the following Delphi Corporation Divisions shall meet the requirements of the **SQ-1000 Supplier Engineering Laboratory Verification and Approval.**

Delphi Electronics and Safety
Delphi Thermal and Interior
Delphi Packard Electric
Delphi Energy and Chassis
Delphi Saginaw Steering

This requirement also applies to **ITT Automotive Division**

Annual Run at Rate is not required for semiconductors for PSW. Annual layout inspection is not required for semiconductor devices.

Visteon Corporation – Specific Requirements

There are no additional customer specific requirements.

Glossary

Captive Assembly/Test Facility	An assembly or test facility that is owned by a semiconductor supplier primarily for internal use.
Design Validation Testing	Early prototype testing to validate design intent. This may include prototype tooling and processes.
Design Qualification Testing	Production intent testing to assure design intent is fully met. This shall include production tooling and processes.
Failure Mode and Effects Analysis (FMEA)	**Design FMEA (DFMEA)** An FMEA which quantifies design related failure modes as a function of probability of occurrence, severity, and detectability. **Process FMEA (PFMEA)** An FMEA that quantifies process parameter related failure modes as a function of probability of occurrence, severity, and detectability.
Gage	Any device used to obtain measurements.
Gage R&R Study	An analysis of measurement system repeatability and reproducibility. For more information, refer to the **Measurement Systems Analysis (MSA)** reference manual.
Golden Units	Master samples or standards generally used for verifying test equipment setup.
Guardband	A tightened offset from a specification limit that accommodates or accounts for a statistically predictable variation.
Maverick Lot	A lot of material whose yield or parametric data indicates a significant statistical departure from typical material. See **AEC-Q002 Guidelines for Statistical Yield Analysis**

Glossary

Nominal Device Limits	Parametric limits established to discard product which is deviant from that seen when process is under control.
Part Average Testing	A statistically based technique for removing parts with abnormal characteristics (outliners) from product being tested. See **AEC-Q001 Guidelines for Part Average Testing.**
Problem Analysis	Team oriented problem solving objectives or methodology. Examples 8D, 7D, or 5 phase.
Process Corners	These are the high and low combinations of interacting processes considered during characterization of a part. Example: Base sheet resistivity and NPN beta. The process corners would be Highp/High B, High p/LoowB, Lowp/LowB, Low p/High B.
Qualification	The series of environmental stress tests intended to validate a device as part of the approval process for use in automotive application.

KEY CONTACTS

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